Real-time simulations of networks of Hodgkin–Huxley neurons using analog circuits

Q. Zoua, Y. Bornatb, J. Tomasb, S. Renaudb, A. Destexheb

a UNIC, CNRS, Gif-sur-Yvette, UPR-2191, France
b IXL, CNRS, ENSEIRB-Université Bordeaux 1, UMR 5818, France

Available online 7 February 2006

Abstract

The traditional dilemma for performing network simulations with analog circuits is the great difficulty of handling the connectivity in hardware. The main problem is that hardware-based connectivity must be built following predefined plasticity and connectivity rules, and that once the hardware is built, it is usually not possible to change its configuration. We show here an alternative system in which the membrane equations are solved in analog ASIC circuits, but the connectivity remains controlled by a digital computer. We illustrate the behavior of this system by comparing the analog simulations with traditional computer simulations of the same models.

1. Introduction

We describe here a platform for simulating networks of neurons based on the Hodgkin–Huxley (HH) formalism and conductance–based synaptic interactions. The system is based on analog integrated circuits (ASICs) which solve the membrane equations of the neurons. Each ASIC neuron is equipped with a leak conductance, the $I_{Na}$ and $I_{Kd}$ voltage-dependent conductances for generating action potentials (HH model), a slow voltage-dependent $K^+$ conductance for spike-frequency adaptation, and two conductance-based synaptic currents that implement kinetic models of glutamate and GABA receptors. The connectivity between the neurons is entirely managed digitally using a computer, which is interfaced in real-time (RT-LINUX) with the board containing the ASIC neurons. We demonstrate here the functionality of this system for small networks of excitatory and inhibitory neurons with excitatory synapses endowed with spike-timing dependent plasticity (STDP) and fixed inhibitory synapses. We compare the behavior of the ASIC-based model with numerical simulations of the same models.

2. Methods

We used a system specifically designed for analog neuron simulations (see scheme in Fig. 1A). This system consisted in custom-designed specific ASICs for simulating conductance-based neuronal models using HH type models. We describe below these models, as well as the architecture of the system and ASIC circuits.

Models implemented. The neuron models implemented on circuits were HH type representations of two main cell classes in cortex, the “regular spiking” (RS) neurons and “fast spiking” (FS) interneurons. All neurons contain an adjustable leak conductance and voltage-dependent Na$^+$ and K$^+$ conductances necessary to generate action potentials. These currents define the FS phenotype for inhibitory neurons. Excitatory RS neurons possess in addition a slow voltage-dependent $K^+$ current responsible...
Fig. 1. Network simulations using analog neurons. (A) Scheme of the system architecture for performing analog simulations. Membrane equations are solved on analog ASIC chips, but the connectivity is handled by a computer in real time. (B) Scheme of the network used as an example. The system was tested using a 8-neuron circuit comprising 6 "regular spiking" (RS) excitatory neurons and 2 "fast spiking" (FS) inhibitory neurons. These neurons were reciprocally connected with excitatory (AMPA, solid lines, maximal conductances of 10 nS) and inhibitory (GABA, dashed lines, maximal conductances of 5 nS) synapses, and each cell received random synaptic activity at both AMPA (gray arrow) and GABA (white arrow) synapses, with maximal conductances of 0.1 and 0.05 mS, respectively. (C) Firing properties of a single ASIC neuron bombarded by random synaptic inputs. Poisson-distributed random synaptic (AMPA) inputs were used at different rates $g_{\text{AMPA}}$ (maximal conductance of 0.1 mS). The raster plots show the spikes produced by the neuron during 10 successive simulations of 1 s, for ASIC (left; 1 kHz sampling frequency) and model (right) simulations. (D) Comparison of firing rates in ASIC and model simulations. The average firing rate was computed from the simulations shown in C, and represented as a function of the mean input rate of the synaptic bombardment. (E) Steady-state synaptic weights in ASIC simulations of the 8-neuron circuit shown in B. Synaptic plasticity (STDP) was incorporated at excitatory synapses from RS to FS cells, and the final weight is shown after 50 s simulation time. The simulation was repeated for different input rates of the random excitatory inputs (from 10 to 100 Hz), while the inhibitory input rate was fixed at 20 Hz. (F) Same model run numerically.
3. Results

ASIC circuits.

Analog-digital interface.

3. Conclusions
The prototype shown here works well, and was also tested in different configurations including recurrent excitatory synapses subject to STDP (Zou et al., submitted). This system is a novel solution to run real-time neuromorphic devices of complex neural models while keeping a modular and dynamic connectivity. Other approaches propose solutions either with less precise neuron models [2], or without programmability at the network level [11].

The main limitation of such a system is that the digital interface must compute synaptic weights in real time, which may represent a difficulty for applying complex plasticity algorithms to large networks. Further work is needed to evaluate the limit of such analog/digital architectures. In parallel, architectural solutions are already studied to process the network connectivity at the hardware level, using reconfigurable digital circuits (FPGA). However, the fact that networks of HH neurons can be simulated in real time opens the possibility of interfacing them with real neurons (see Ref. [7]). Another interesting approach will be to evaluate how neuron variability, emulated here by the dispersion in the ASICs characteristics, influences the activity patterns at the network level.

Acknowledgements

This work was supported by CNRS, HFSP and the European Community (IST-2001-34712 and IST-2005-015879).

References

4. A. D s h , Z.F. , . . . W s A s d s l b s s , , s d C d . 6 (1994) 14 18.
5. A s , C s s d l d C d . 9 (1997) 1179 1209.
6. A. h , A.F. d , A d s b , s d s d , s . . , 117 (1952) 500 544.
7. G. s , . d s s A s D s D b , B F b , s s . s , 161 (2004) 57 69.
8. A s A , B s d , B d s s , D s C d , D s s DC . 2003, 2003.
10. A h , s . B s d A h b s d b s s . A . . . C b s , D h , A d d s d h h h , s s EEE s E B C . 51 (2004) 342 354.